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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/526,394	HOWELL ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,6,9,10,13,22,24 and 26-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,6,9,10,13,22,24 and 26-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/16/03 has been entered. An action on the RCE follows.

2. The amendment filed on 09/22/03 has been entered.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 6, 13 and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

A. Claim 6, line 13 recites the limitations "wherein said second metal plug has a thickness sufficient to consume tin diffusing from said solder bump".

As described in the specification, the second copper film 36 (see copper plug 2 in Fig. 3) is deposited with sufficient thickness to be at least coplanar with the top of the passivation films (specification page 9, lines 10-12). However, the description does not disclose the thickness of the second plug or what is considered as being the sufficient thickness of the second metal plug which consumes tin diffusing from the solder bump.

B. Claim 13, lines 14-17 recite the limitations "wherein said second plug forms sufficient intermetallics with elements diffusing from said solder bump", and "wherein said second plug has a thickness sufficient to consume tin diffusing from said solder bump".

As described in the specification, the second copper film 36 (see copper plug 2 in Fig. 3) is deposited with sufficient thickness to be at least coplanar with the top of the passivation films (specification page 9, lines 10-12). However, the description does not disclose the thickness of the second plug or what is considered as being the sufficient thickness of the second metal plug which consumes tin diffusing from the solder bump and forms sufficient amount of intermetallics.

C. Claim 23, lines 8-10 recite the limitations "forming a conductive structure that includes a given species including tin" and "said second layer of copper having a

thickness sufficient to form intermetallics with said species diffusing from said conductive structure".

As described in the specification, the copper plug 24 is recessed 1000-10000 angstroms to form a recessed plug 34 (specification page 9, line 7). However, the it does not disclose the thickness of the second layer of copper in the recessed plug 34 or what is considered as being the sufficient thickness of the second layer of copper which forms intermetallics with the species diffusing from the conductive structure.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, 29 and 30 insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. (US Pat. 5290732) in view of Cohen (US Pat. 6136707) and admitted prior art (APA).

Regarding claim 6, Kumar et al. disclose a metallurgical/conductive structure in an integrated circuit (IC) chip having underlying circuitry/internal components within an exterior covering comprising:

- a first layer/line/metal pad/internal component (14b in Fig. 10) on the chip/substrate
- a passivation/insulating layer (16b in Fig. 10)
- a via/hole (Fig. 10) through the passivation layer extending to the first layer/metal pad/line
- a barrier layer/first barrier layer lining the via (18b in Fig. 10), and
- a metal plug/bump/second layer (40b in Fig. 10; 40 in Fig. 9) in the via above the barrier layer wherein the metal plug/bump, barrier layer and the passivation layer form a planar exterior surface of the metallurgical structure,
- the metal plug/bump being of predetermined thickness and being made of material such as copper (Col. 5, line 44)
- solder bump/connector/conductive structure (44 in Fig. 10; Col. 6, line 10) comprising a tin/lead alloy, the solder bump being in direct contact with the
- conductive/metal plug (40b in Fig. 10) and the bump being on the planar exterior surface

(Fig. 10; Col. 5, line 23- Col. 6, line 15; Fig. 5-10; Col. 3-12).

Kumar et al. further disclose the conductive structure having the solder bump/connector where the barrier layer comprises an adhesion/barrier material such as Ti, TiN, TaN, nickel, etc. with a copper plug of predetermined/sufficient thickness

being used to reduce/prevent the diffusion of elements/species/metals such as tin, present within the solder bump/conductive structure into the metal line to provide low contact resistance and improved adhesion/reliability (Col. 3, line 36-68; Col. 3-6).

Kumar et al. fail to teach:

a) a second barrier layer above the first metal plug and a second metal plug above the second barrier layer wherein the second metal plug and the first and second barrier layers form a planar exterior surface, and

b) the second metal plug having a thickness sufficient to consume tin diffusing from the solder bump.

a) Cohen teaches a multilayered interconnect structure (Fig. 3 and 4) comprising a plurality of barrier/adhesion, seed and metal plug layers having an optimized/sufficiently thick seed/plug layers to provide an improved adhesion, reduced out-diffusion of copper/copper intermetallic compounds and low resistance (Col. 1, lines 35-55; Col. 3, lines 5-30; Col. 8, line 55; Col. 6, line 65- Col. 9, line 2). Cohen teaches such structure comprising a second seed/barrier layer (128 in Fig. 4; Col. 8, line 7; Col. 9, line 1) above the first non conformal seed layer/metal plug layer (126 in Fig. 4) and a second metal fill/plug (130 in Fig. 4) above the second seed/barrier layer, wherein the second metal fill/plug and the first and second barrier/seed layers form a planar exterior surface (see Fig. 4; Col. 6, line 65- Col. 9, line 2).

b) Furthermore, Cohen teaches using the second metal fill/plug layer of copper being of sufficient thickness or with excess to fill an opening of the trench/plug having a dimension of about 1800 angstroms (Col. 6, lines 20-32).

It is well known in chip packaging and interconnection technology art that copper readily reacts and forms intermetallics with elements such as tin from the solder (see admitted prior art- specification page 3, line 12; pages 3 and 4).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second barrier layer above the first metal plug and a second metal plug above the second barrier layer wherein the second metal plug and the first and second barrier layers form a planar exterior surface, and the second metal plug having a thickness sufficient to consume tin diffusing from the solder as taught by Cohen and APA so that the desired electrical resistance and the protection/barrier against the diffusion of intermetallics and the interconnect reliability can be improved in Kumar et al's structure.

Regarding claim 29, Kumar et al., Cohen and APA teach substantially the entire claimed structure as applied to claim 6 above, wherein Kumar et al. further teach solder bump (44 in Fig. 10; Col. 6, line 10) comprising the tin/lead alloy.

Regarding claim 30, Kumar et al., Cohen and APA teach substantially the entire claimed structure as applied to claim 6 above, except the second metal plug forming sufficient intermetallics with elements diffusing from the solder bump so as to prevent the elements from penetrating through the first and second barrier layers into the metal line.

Cohen further teaches using the second metal fill/plug layer of copper being of sufficient thickness or with excess to fill an opening of the trench/plug having a dimension of about 1800 angstroms (Col. 6, lines 20-32).

It is well known in chip packaging and interconnection technology art that copper readily reacts and forms intermetallics with elements such as tin from the solder (see admitted prior art- specification page 3, line 12; pages 3 and 4).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second metal plug forming sufficient intermetallics with elements diffusing from the solder bump so as to prevent the elements from penetrating through the first and second barrier layers into the metal as taught by Cohen and APA so that the desired electrical resistance and the protection/barrier against the diffusion of intermetallics and the interconnect reliability can be improved in Cohen, APA and Kumar et al's structure.

7. Claims 9, 13, 22, 23, 24, 26, 28 and 31, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. (US Pat. 5290732) in view of Cohen (US Pat. 6136707), admitted prior art (APA) and Zhao et al. (US Pat. 5674787).

Regarding claims 13 and 9, Kumar et al. disclose a metallurgical/conductive structure in an integrated circuit (IC) chip having underlying circuitry/internal components within an exterior covering comprising:

- a first layer/line/metal pad/internal component (14b in Fig. 10) on the chip/substrate
- a passivation/insulating layer (16b in Fig. 10)
- a via/hole (Fig. 10) through the passivation layer extending to the first layer/metal pad/line
- a barrier layer/first barrier layer lining the via (18b in Fig. 10), and
- a metal plug/bump/second layer (40b in Fig. 10; 40 in Fig. 9) in the via above the barrier layer wherein the metal plug/bump, barrier layer and the passivation layer form a planar exterior surface of the metallurgical structure,
- the metal plug/bump being of predetermined thickness and being made of material such as copper (Col. 5, line 44)
- solder bump/connector/conductive structure (44 in Fig. 10; Col. 6, line 10) comprising a tin/lead alloy, the solder bump being in direct contact with the
- conductive/metal plug (40b in Fig. 10) and the bump being on the planar exterior surface

(Fig. 10; Col. 5, line 23- Col. 6, line 15; Fig. 5-10; Col. 3-12).

Kumar et al. further disclose the conductive structure having the solder bump/connector where the barrier layer comprises an adhesion/barrier material such as Ti, TiN, TaN, nickel, etc. with a copper plug of predetermined/sufficient thickness being used to reduce/prevent the diffusion of elements/species/metals such as tin, present within the solder bump/conductive structure into the metal line to provide low contact resistance and improved adhesion/reliability (Col. 3, line 36-68; Col. 3-6).

Kumar et al. fail to teach:

a) the first plug, the second plug and the internal components comprising the same material, and

b) the second metal plug having a sufficient thickness to consume tin diffusing from the solder bump and forming sufficient intermetallics with elements diffusing from the solder bump so as to prevent the elements from penetrating through the first and second barrier layers into the internal components.

a) Cohen teaches a multilayered interconnect structure (Fig. 3 and 4) comprising a plurality of barrier/adhesion, seed and metal plug layers having an optimized/sufficiently thick seed/plug layers to provide an improved adhesion, reduced out-diffusion of copper/copper intermetallic compounds and low resistance (Col. 1, lines 35-55; Col. 3, lines 5-30; Col. 8, line 55; Col. 6, line 65- Col. 9, line 2). Cohen teaches such structure comprising a second seed/barrier layer (128 in Fig. 4; Col. 8, line 7; Col. 9, line 1) above the first non-conformal seed layer/metal plug layer comprising copper (126 in Fig. 4; Col. 8, line 7) and a second metal fill/plug (130 in Fig. 4) above the second seed/barrier layer, wherein the second metal fill/plug and the first and second barrier/seed layers form a planar exterior surface (see Fig. 4; Col. 6, line 65- Col. 9, line 2).

Zhao et al. teach using a conductive structure having a metal plug and a metal line where the metal plug (23 in Fig. 6) and the metal line (11 in Fig. 6) comprise conventional material such as copper (23/11 in Fig. 6; Col. 5, line 22; Col. 7, line 25).

b) Cohen further teaches using the second metal fill/plug layer of copper being of sufficient thickness or with excess to fill an opening of the trench/plug having a dimension of about 1800 angstroms (Col. 6, lines 20-32).

It is well known in chip packaging and interconnection technology art that copper readily reacts and forms intermetallics with elements such as tin from the solder (see admitted prior art- specification page 3, line 12; pages 3 and 4).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the second plug and the internal components comprising the same material such as copper as taught by Cohen and Zhao et al. and the second metal plug forming sufficient intermetallics with elements diffusing from the solder bump so as to prevent the elements from penetrating through the first and second barrier layers into the internal components as taught by Cohen and APA so that the desired electrical resistance can be achieved and the barrier against the diffusion of intermetallics can be improved in Kumar et al's structure.

Regarding claims 23 and 28, Kumar et al. disclose a metallurgical/conductive structure in an integrated circuit (IC) chip having underlying circuitry/internal components within an exterior covering comprising:

- a first layer/line/metal pad/internal component (14b in Fig. 10) on the chip/substrate
- a passivation/insulating layer (16b in Fig. 10)
- a via/hole (Fig. 10) through the passivation layer extending to the first layer/metal pad/line
- a barrier layer/first barrier layer lining the via (18b in Fig. 10)

- a metal plug/bump/second layer (40b in Fig. 10; 40 in Fig. 9) in the via above the barrier layer wherein the metal plug/bump, barrier layer and the passivation layer form a planar exterior surface of the metallurgical structure,
- the metal plug/bump being of predetermined thickness and being made of material such as copper (Col. 5, line 44), and
- solder bump/connector/conductive structure (44 in Fig. 10; Col. 6, line 10) comprising a tin/lead alloy, the solder bump being in direct contact with the conductive/metal plug (40b in Fig. 10) and the bump being on the planar exterior surface

(Fig. 10; Col. 5, line 23- Col. 6, line 15; Fig. 5-10; Col. 3-12).

Kumar et al. further disclose the conductive structure having the solder bump/connector where the barrier layer comprises an adhesion/barrier material such as Ti, TiN, TaN, nickel, etc. with a copper plug of predetermined/sufficient thickness being used to reduce/prevent the diffusion of elements/species/metals such as tin, present within the solder bump/conductive structure into the metal line to provide low contact resistance and improved adhesion/reliability (Col. 3, line 36-68; Col. 3-6).

Kumar et al. fail to teach:

a) the first layer and the second layer being copper, and

b) the third layer of copper being formed on the second barrier layer, the second copper layer having a sufficient thickness to form intermetallics with the species diffusing from

the conductive structure and to adhere to the conductive structure, so as to prevent the elements from penetrating through the first barrier layer into the first layer of copper.

a) Cohen teaches a multilayered interconnect structure (Fig. 3 and 4) comprising a plurality of barrier/adhesion, seed and metal plug layers having an optimized/sufficiently thick seed/plug layers to provide an improved adhesion, reduced out-diffusion of copper/copper intermetallic compounds and low resistance (Col. 1, lines 35-55; Col. 3, lines 5-30; Col. 8, line 55; Col. 6, line 65- Col. 9, line 2). Cohen teaches such structure comprising a second seed/barrier layer/second layer (128 in Fig. 4; Col. 8, line 7; Col. 9, line 1) above the first non-conformal seed layer/metal plug layer comprising copper (126 in Fig. 4; Col. 8, line 7) and a metal fill/plug/third layer (130 in Fig. 4) above the second seed/barrier layer, wherein the second metal fill/plug and the barrier layers/seed layers and metal plug/fill layers form a planar exterior surface (see 118/126/128 and 130 in Fig. 4; Col. 6, line 65- Col. 9, line 2).

Zhao et al. teach using a conductive structure where a metal plug/second layer (23 in Fig. 6) and a metal line/first layer comprises a conventional material such as copper (23/11 in Fig. 6; Col. 5, line 22; Col. 7, line 25).

b) Cohen further teaches the non-conformal seed layer/metal plug layer of copper (126 in Fig. 4) being of predetermined/sufficient thickness ranging from 100-2000 angstroms (Col. 7, lines 52-58) or having a plurality of such layers including layers having higher thickness (Col. 8, lines 52-60).

It is well known in chip packaging and interconnection technology art that copper readily reacts and forms intermetallics with elements such as tin from the solder (see admitted prior art- specification page 3, line 12; pages 3 and 4).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the first layer and the second layer being copper as taught by Cohen and Zhao et al. and the third layer of copper being formed on the second barrier layer, the second layer of copper having a thickness sufficient to form intermetallics with species diffusing from the conductive structure and to adhere to the conductive structure, so as to prevent the species from penetrating through the first barrier layer into the first layer of copper as taught by Cohen and APA so that the desired electrical resistance and the barrier against the diffusion of intermetallics can be improved in Kumar et al's structure.

Regarding claims 22, 24 and 26, Kumar et al., Cohen, APA and Zhao et al. teach substantially the entire claimed structure as applied to claims 13 and 23 above, wherein Kumar et al. further teach the conductive structure comprising the solder ball/connector made of the tin/lead alloy having elements/species such as tin (44 in Fig. 10; Col. 6, line 10).

Regarding claim 31, Kumar et al., Cohen, APA and Zhao et al. teach substantially the entire claimed structure as applied to claim 23 above, wherein Kumar et al. further teach the metallurgical structure being substantially coplanar/planarized (see Fig. 10).

9. Claim 2 insofar as being in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. (US Pat. 5290732), Cohen (US Pat. 6136707) and APA as applied to claim 6 above, and further in view of Zhao et al. (US Pat. 5674787).

Regarding claim 2, Kumar et al., Cohen and APA teach substantially the entire claimed structure as applied to claim 6 above, except the metal line and the first and second metal plugs comprising the same material such as copper.

Cohen further teaches using the first seed/metal plug layer being of copper (126 in Fig. 4; Col. 8, line 7) and the second metal fill/plug layer being of copper (130 in Fig. 4; Col. 6, lines 30).

Zhao et al. teach using the metal plug (23 in Fig. 6) and the metal line comprising conventional material such as copper (23/11 in Fig. 6; Col. 5, line 22; Col. 7, line 25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal line and the first and second metal plugs comprising the same material such as copper as taught by Cohen and Zhao et al. so that the desired electrical resistance can be achieved and the barrier against the diffusion of intermetallics can be improved in APA, Cohen and Kumar et al's structures.

10. Claim 3 insofar as being in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. (US Pat. 5290732), Cohen (US Pat. 6136707) and APA as applied to claim 6 above, and further in view of Mori et al. (US Pat. 6335570).

Regarding claim 3, Kumar et al., Cohen and APA teach substantially the entire claimed structure as applied to claim 6 above, except the second barrier layer comprising one or more layers of Ti, TiN, Ta and TaN .

Mori et al. teach a multilevel copper plug structure to provide an improved protection against diffusion of copper compounds/intermetallics into underlying insulating layers and metalization, the structure comprising a plurality of barrier layers including the first and second barrier layers (4 and 42 respectively in Fig. 18; Col. 6, line 17, Col. 9, line 57) comprising TaN .

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the first and second barrier layers comprising one or more layers of Ti, TiN, Ta and TaN as taught by Mori et al. so that the desired electrical resistance can be achieved and the protection/barrier against the diffusion of intermetallics and the dielectric layer integrity can be improved in Cohen, APA and Kumar et al's structure.

11. Claims 10 and 27, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. (US Pat. 5290732) in view of Cohen (US Pat. 6136707), admitted prior art (APA) and Zhao et al. (US Pat. 5674787) as applied to claims 13 and 23 respectively above, and further in view of Mori et al. (US Pat. 6335570).

Regarding claims 10 and 27, Kumar et al., Cohen, APA and Zhao teach substantially the entire claimed structure as applied to claims 13 and 23 respectively above, except the second barrier layer comprising one or more layers of Ti, TiN, Ta and TaN .

Mori et al. teach the multilevel copper plug structure to provide an improved protection against diffusion of copper compounds/intermetallics into underlying insulating layers and metalization, the structure comprising a plurality of barrier layers including the first and second barrier layers (4 and 42 respectively in Fig. 18; Col. 6, line 17, Col. 9, line 57) comprising TaN .

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the first and second barrier layers comprising one or more layers of Ti, TiN, Ta and TaN as taught by Mori et al. so that the desired electrical resistance can be achieved and the protection/barrier against the diffusion of intermetallics and the dielectric layer integrity can be improved in Cohen, APA and Kumar et al's structure.

Response to Arguments

12. Applicant's arguments with respect to claims 2, 3, 6, 9, 10, 13 and 22, 24 and 26-31 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-305-1690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

Nitin Parekh
11-30-03

EDDIE LEE
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